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ABSTRACT

During this quarter further investigations of alternative designs for the Lincoln Training System LTS-4 project's features and subsystems continued. Software efforts proceeded concurrently in three areas: 1) system architecture, monitor, and input/output programs; 2) a new version of the Lincoln Terminal Language, LTL-2; and 3) programs to apply LTL to author needs. Hardware developments resulted in the design and installation of a new film gate in the image rotator and in the implementation of a new vernier positioning technique. In addition, most of the parts for the rotating microscope selector/reader were released for fabrication and the self-processor interface was nearly completed. Finally, considerable progress was made on the development of system software utilizing the MCS-4 simulator. (Author/PB)

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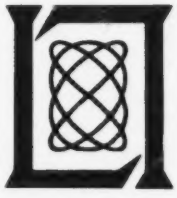

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ABSTRACT

Work during this quarter has concentrated on further investigations of alternative designs for LTS-4 features and subsystems. A new film gate was designed and installed in the image rotator, and a new vernier positioning technique was implemented. Most of the parts for the rotating microscope selector/reader have been released for fabrication.

The self processor interface is nearing completion, and considerable progress has been made on system software utilizing the MCS-4 simulator. A new version of the author program language has been developed, and modifications of an LTS-3 to a stand-alone version for use in an author support facility are in progress.

15 June 1973

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EDUCATIONAL TECHNOLOGY PROGRAM

I. LTS-4 SOFTWARE DEVELOPMENT

With completion of the experimental tests of the LTS concept and in anticipation of an extensive field trial of stand-alone terminals, software efforts have been concentrated on development of an author language and programs. New requirements evolved from the experience in the recent trials at the Keesler School for Applied Aerospace Science of the Air Force. Also, new advantages and limitations have been imposed by stand-alone operation and by the choice of the MCS-4 computer for both interim and prototype terminals. Design and implementation in three areas have proceeded concurrently: (a) system architecture, monitor, and I/O programs, (b) LTL-2, a new version of the Lincoln Terminal Language, and (c) programs to apply LTL to author needs.

A. MCS-4 System Architecture

The MCS-4 is a machine with a 4-bit word length. It has 4096 bytes of read-only program space, 512 bytes of MAIN read-write memory, 128 bytes of STATUS read-write memory, and 16 4-bit general registers. The cycle time is 10.8 μsec.

The LTL processor is laid out in the MCS-4 as shown in Fig. 1. The memory of the LTL interpreter includes four pages of R-W (read-write) memory and twelve more of R-O (read-only). There are 128 bytes of 8 bits each per page. Data and program can be loaded to the R-W space from fiche or from a teletype. Special tables and procedures associated with each audio/visual

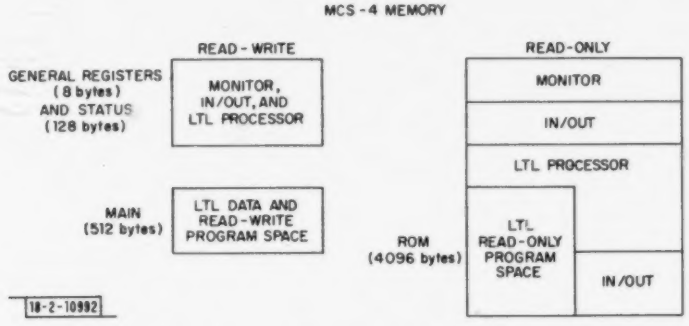

Fig. 1. Layout of space for realization of Lincoln Terminal Language on MCS-4 computer.

frame are accommodated in this manner. The R-O space includes subroutines for device control, I/O operations, keyboard interpretation, and maintenance checkout. The content of only a few of the read-only memory chips in the MCS-4 determines the user capacities of the terminal. These few may be changed readily to accommodate varied applications of the device. Thus, the over-all design permits maximum flexibility of the machine.

B. Lincoln Terminal Language (LTL-2)

A new version of the author program language has been programmed on the MCS-4 simulator, implemented on a DEC PDP-8 computer. The goal was to provide within the MCS-4 (itself a

TABLE I

LIST OF LTL OPERATORS

Algebraic	ADD A_i B_i	$B_i = B_i + A_i$, binary
	ADV A_i B_i	$B_i = B_i + A_i$, decimal
	SUB A_i B_i	$B_i = B_i - A_i$, binary
	SBV A_i B_i	$B_i = B_i - A_i$, decimal
	SUM A_i B_j	B_1 = sum of A_i B_o = overflow of sum
	SET K A_i	A_i = k, k is a constant
	INT A B_i	$B_1 = A$, $B_2 = A + 1$, $B_3 = A + 2, \ldots$
	INC A	Increment byte A
	DEC A	Decrement byte A
	SRL A	Shift byte A left
	SRR A	Shift byte A right
Bit	STB N A	Bit N of A set to one
	CLB N A	Bit N of A set to zero
	PCK A_i B_i	Pack characters of A (4-bit) to bytes of B (8-bit)
	UPK A_i B_i	Unpack bytes of A to characters of B
	MSK A B_i	AND each byte of B_i with A
	CPY L N A_i	Copy from L N bytes to A_i
	XFR A_i B_i	Transfer bytes A_i to B_i
Skip	SKB N A	Skip next operation if Nth bit of A is one
	SKR R A_i B_i	Skip if A_i R B_i for all i, where R is $<$, $=$, $>$, $\leqslant$, $\neq$, $\geqslant$
	SKL R A_i B_i C_i	Skip if A_i R B_i and B_i R C_i
Jump	JMP L	Jump to location L
	JMS L	Jump to subroutine at L
	RET	Return from subroutine

tedious environment for author programming) an interpretive, higher level language geared to LTS application. A number of requirements have been met. LTL is a language for manipulation of byte strings and short data tables. It is slow by computer standards, but fast enough to service human responses. The operations are designed to be powerful, i.e., easy to relate operationally to one another to achieve an interpretive function, and yet also easy to understand and write.

The operators are listed in Table I. Many author functions can be served by operating on short strings of bytes. Strings are subscripted values, i.e., A_i, B_i, C_i of 1 to 8 bytes in length. (The length not indicated is incorporated in the operator bytes.) A, B, C may be direct references to data in Page 0 or may contain a bit indicating indirect reference via Page 0 to data in 0 or 1.

The language is convenient from a system software viewpoint. A simple assembler, like DEC MACRO-8, is easily adapted to LTL assembly. The conventions are few in number. Paging of program references is avoided: LTL will run not only across page boundaries but, since the operators are read-only, across the RAM/ROM boundary. Flexibility is achieved by the fact that address constants of program located in Page 0 or 1 may be treated as data. As a final comment, runs on the simulator show that average speed of LTL on the MCS will be one operation per 2 to 3 msec, within limits of 1 to 13 msec.

C. Author Logic

Tutorial interaction is supported by means of author logic, which is read into RAM at the start of each frame. Logic comprises either the standard list, or the standard list followed by successive special lists which determine how student responses are interpreted. In addition to logic, the data read in from the fiche can contain programs that are intended for temporary use during the frame.

The standard list indicates:

(1) The location of the frame in the lesson.

(2) Whether the frame is accessible to the student when he scans through the lesson using the BACK, FORTH, and frame SELECT keys.

(3) The number of scheduled audio pauses (message interruptions which are terminated by the student when he is ready to proceed).

(4) Whether the frame ends automatically when the last audio pause occurs.

(5) The number of the student record that is incremented a specified amount, and whether this record or all the student's records (their sum) will be evaluated against a specified criterion.

(6) The next frame if the student requests additional instruction using the HELP key.

(7) The next frame if the student may proceed without entering an informational response.

Informational responses by the student employ one or more numeric keys (i.e., 0-9, the minus sign, and the decimal point) followed by a GO-ON keypress. Special programs which evaluate these responses are written in LTL-2. The programs are invoked and directed by the parameters in author logic, and a number of response-evaluation programs can be run successively

TABLE II

ORGANIZATION OF LOGIC FOR MULTIPLE-CHOICE RESPONSES

CHOOSE	/evaluation 1 – first choice
limit	/number of alternatives
correct	/correct alternative
CHOOSE	/evaluation 2 – second choice
•••	
CHOOSE	/evaluation 3 – third choice
•••	
FDBK3E	/assign feedback for three evaluations
frame for all +	/all correct
frame for 1 –	/first only incorrect
frame for 2 –	/second only incorrect
frame for 3 –	/third only incorrect
frame for 3 +	/third only correct
frame for 2 +	/second only correct
frame for 1 +	/first only correct
frame for other	/default transfer and none correct

on one frame (cf. Tables II and III). The programs require the capacity to set pointers easily. This is accomplished with one of the LTL-2 operators, INT, which causes a vector of integers to be added to a base.

Each program identification code directs the author system to the appropriate special program, which is executed once for the corresponding list in logic. Then pointers are set to point to the next list in logic, and the next special program is invoked. Schematic illustrations are provided for two basic kinds of response formats: multiple-choice (Table II) and constructed (Table III).

In the multiple-choice example, the student is expected to make three successive choices from three sets of alternatives. If the student does not make three responses within the specified limits, the red error light comes on and the response is cleared. Responses are evaluated in succession with reference to the corresponding list in logic. Finally, the author system runs the feedback program, which assigns the next frame depending on the pattern of correct responses the student made. In the example, FDBK3E is used because three special programs evaluated the correctness of the student's response.

In the constructed-response example, the student is expected to enter a signed numeric response, which represents the result of a calculation. When he presses GO-ON, this response is evaluated with reference to two criterion responses, each of which is specified by a pair of limits. As Table III shows, the criterion values are kept in separate RAM words to facilitate the evaluation. Whether the student's response falls within the first or the second pair of limits is determined easily with the skip-on-limits operator. After both limits have been applied,

TABLE III

ORGANIZATION OF LOGIC FOR CONSTRUCTED RESPONSES

NUMBER	/evaluation 1 – first constructed
sign	/+ or –
exponent	/power of 10; upper limit of first criterion for evaluation
digit 1	
digit 2	
digit 3	
exponent	/power of 10; lower limit of first criterion for evaluation
digit 1	
digit 2	
digit 3	
NUMBER	/evaluation 2 – first constructed
•••	
WAIT	/clear response; wait for next response
CHOOSE	/evaluation 3 – first choice
limit	/number of alternatives
correct	/correct alternative
FDBK3E	/assign feedback for 3 evaluations
frame for all +	/all correct
frame for 1 –	/first only incorrect
frame for 2 –	/second only incorrect
frame for 3 –	/third only incorrect
frame for 3 +	/third only correct
frame for 2 +	/second only correct
frame for 1 +	/first only correct
frame for other	/default transfer and none correct

the WAIT program causes the system to wait for the next response – in this case a multiple-choice response (e.g., choice of a unit of measurement). Finally, FDBK3E assigns the feedback frame as a function of all the response evaluations made during the frame.

II. LTS-4 HARDWARE DEVELOPMENT

Modifications to the image rotator breadboard fiche handling subsystem were installed and checked out during this quarter. The control circuits were modified to accommodate row fiducial marks for coarse positioning. Other modifications include the design and installation of a new film gate, the addition of a fiber light guide illuminator, and the implementation of the vernier positioning technique described in the previous Quarterly Technical Summary. Final system characterization studies are under way, and the data collected on the various subsystems will be used as a reference for the data collected during cycle tests, which are scheduled for early summer.

The mechanical and electrical design of the rotating microscope microfiche selector/reader is in the final stages, and most of the parts have been released for fabrication. Assembly and checkout of several reader subassemblies have been initiated.

Design of the self processor interface is nearing completion. This interface will permit the SIM4-02 to drive either the LTS-3/S, image rotator, or rotating microscope breadboards for the purpose of cycle testing. The SERIN program to process up to 12,000 bits of raw data from the audio spiral has been debugged. This provides the system with the capability of loading the entire microprocessor random-access memory from a single frame.

A. Image Rotator System

A fiche selector mechanism was added to the image rotator reader. This mechanism is based on the design of the MTC reader and has the following features.

(1) A 30-fiche cassette holds each fiche in its own envelope.

(2) The fiche is selected by a unique tab which is struck by a solenoid-operated hammer.

(3) Edge rollers made of stacked-O-rings drive the fiche to the main drive rollers. The edge rollers are then displaced laterally to permit the fiche to be moved by the main rollers only.

(4) The fiche is moved to any row by a pair of geared rubber rollers.

(5) When the fiche has been retracted as far back into the cassette as the main rollers and edge rollers will permit, it is moved the rest of the way by a pair of solenoid-driven return kickers.

(6) A separate stepper motor is used to drive the edge rollers, allowing greater independence in the drive systems.

The air gate on the image rotator reader has been replaced with a glassless pressure gate, similar in action to the gate in the LTS-3. The surfaces touching the fiche envelope are coated with teflon.

The quartz-halogen lamp has been replaced by a fiber optics system. A bifurcated pseudo-random fiber bundle is used. The mounts for the bundles have been designed to give three degrees of freedom for adjusting the illumination uniformity.

A mount permitting fine adjustment in X, Y, and rotation, of the X-Y diode used for vernier centering was installed. The North mark coding system was changed to develop 2-Hz reference signals for the vernier positioning subsystem.

A new DC servo motor and amplifier were installed in the radial tracker which decreased the reset time to less than 0.75 sec. Development continues toward an optimum loop which will initially have a wideband Type I loop for reliable acquisition of a one-revolution lead in spiral, followed by a reduced bandwidth Type I or Type II loop having sufficient gain at 2 Hz to track the modulated spiral in the presence of expected film position errors, lamp output variations, film defects, and mechanical wear.

The coarse row positioning system for the fiche has been substantially upgraded with the addition of a more reliable and accurate film fiducial mark sensor, the addition of row fiducial marks on the film, and the implementation of control circuits to detect and acquire the row fiducial marks. The search algorithm for coarse row positioning is simply one of counting the row fiducial marks during a high-speed access, stopping after the mark is detected, and then backing up to that mark at a lower speed. The present high speed is about 80 mm/sec and the current low speed is 2.5 mm/sec. At speeds above 100 mm/sec, film slip occurs. This slip is dependent solely on the roller drive system and is not influenced by the cassette, gate, or edge rollers. Initial measurements show that the short-term repeatability for a single frame access is ±0.04 mm, and for a single fiche the total frame-frame variation due to inaccuracies in film production is ±0.18 mm. Efforts are under way to upgrade the roller drive system to obtain increased speed without slipping.

A preliminary study was made to determine the amount of column skew. The variation in the average skew from one end of the cassette to the other was less than 0.08 mm while the worst peak-to-peak variation for a single fiche-to-fiche position was ±0.10 mm.

The X-Y position sensing technique described in the previous Quarterly Technical Summary has been installed and is being evaluated. A clear boresight centering target on a black background (as opposed to the dark boresight of LTS-3) is now being used in order to minimize offsets in the system due to light gradients across the increased acquisition area of the diode. The acquisition range in both column and row is in excess of ±1 mm. The current fine X-Y positioning rates are 2.5 mm/sec for row and 1.5 mm/sec for column. The basic speed limitation is imposed by the open-loop response of the lens motor system which limits the closed-loop positioning speed to 1.5 mm/sec.

The current X-Y system accuracy averages well under 0.1 mm. However, with the use of stepper motors having steps of 0.06 mm and 0.04 mm in each axis, the accuracy is limited to 0.08 mm. The residual error due to Dove misalignment is slightly in excess of 0.025 mm. Diode position drift appears to be less than 0.25 mm, and amplifier/diode drift appears to be less than 0.012 mm over a period of several weeks.

Modifications now under way include replacing the stepper motors with DC servo motors to improve resolution, reducing the peak 0.08-mm quantization error, and improving response time. The other sources of error are being monitored for long-term effects.

The effect of gate closing on X-Y accuracy was studied. The uncorrected error due to film curl, caused by gate closure, is of the order of 0.012 mm, and in the current system this is reduced substantially by X-Y correction during the gate closing cycle.

An initial investigation has been made of noise due to the cassette film envelopes. Measurements have been made to determine the effect of the various components of the fiche manipulation system on scratches. The preliminary conclusions are:

(1) The main source of envelope scratching is caused by the other envelopes in the cassette.

(2) The current envelopes cause an increase in the system noise level of 6 dB and a 3-dB attenuation of light level.

(3) Noise due to scratching of the envelopes after 100 operations is of the same order of magnitude as the initial film noise.

Based on these preliminary measurement results, it appears that the current envelopes are inadequate for LTS-4 operation. The main defect is the increase in initial noise level which results in degraded audio quality. Other but less serious defects are the attenuation of the envelope and its tendency to scratch the other envelopes and the film within the envelope. Three techniques for improvement of the current envelope problems are suggested:

(1) Attachment of fiche to upper part of envelope only,
(2) Attachment of fiche to envelope with cut-out over audio spirals,
(3) Better envelope material.

Each of these techniques will be explored with the issues of production, mechanical handling, and scratches being given detailed study.

B. Rotating Microscope Reader System

In the rotating microscope reader, the microfiche is scanned directly by a microscope mounted on a rotating frame. The microscope is free to swing in a radial arc and tracks the audio spiral with a linear translator servo assembly. A small periscope prism is used to permit the microscope to be located at a practical distance from the axis of rotation. The system is being implemented with an Optical Sensor Assembly (OSA), 4× magnification, and an LTS-3 condenser system. In this case the microscope is used in its normal mode. Instead of an eyepiece relaying the image into an eye, the OSA is placed in the image plane. Later this reader will be implemented with the light path reversed. The OSA will be replaced by a 900-nm Light Emitting Diode Assembly (LEDA), while the condenser system will be replaced by a large area photo diode detector, as shown in Fig. 2. The LEDA is split into two segments that straddle the track. Light collected during alternate pulse periods is summed to obtain audio, and the difference provides an error signal for the microscope radial servo motor.

The parts for the rotator assembly have been received and assembled. Testing will begin by the end of June. The design of the fiche handling subsystem for this unit is complete. This subsystem differs from the unit now implemented for the image rotator reader in the following respects:

(1) Row drive is accomplished with a DC servo motor driving both the main and edge rollers. A pair of opto-electronic sensors provides the servo signals for row selection.

(2) Column selection is implemented by moving the entire fiche select mechanism to one of three positions. This is accomplished with a three-position cam driven by a DC

servo motor, electrically similar to the row drive motor. The column change time will be constant, since any cam position selected is only one position away.

(3) The fiche select solenoid is mounted on a carriage driven by a threadless screw actuator and DC servo motor. A potentiometer sensor driven by a cable indicates the position of the select solenoid.

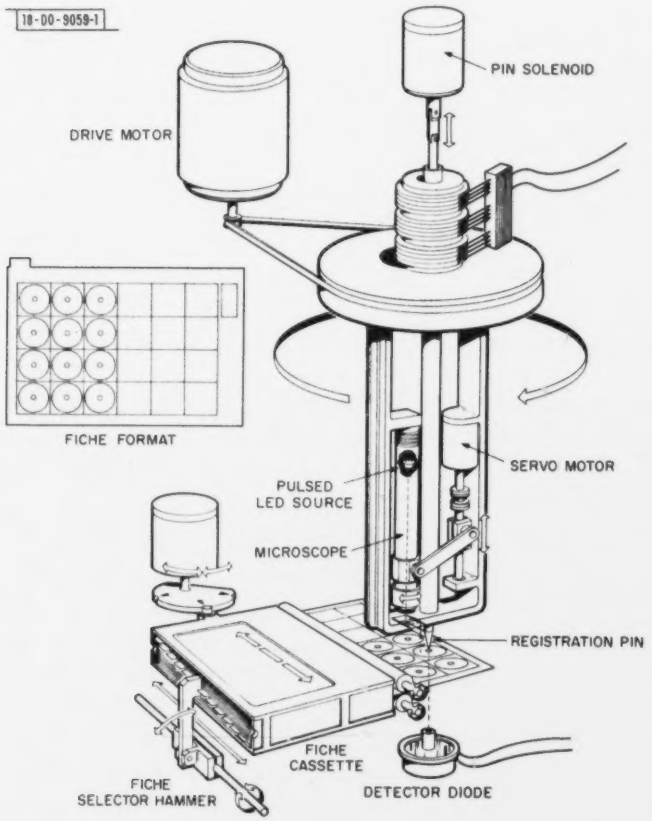

Fig. 2. Rotating microscope reader.

The control circuits for the electro-optical-mechanical components in the selector-reader are implemented with T^2L logic and linear integrated circuits. Functional control signals from the Universal Terminal Tester (UTT) cause the control logic to cycle terminal components through detailed electro-optical-mechanical events, such as fiche selection, frame selection, etc. The commands may be issued by either the UTT manual keyboard or by the computer, as shown in Fig. 3.

The fiche selection servo positions the select hammer by comparing an analog reference voltage derived from the fiche number to a voltage derived from the fiche select potentiometer. When the two voltages are equal, the hammer is actuated, strikes a tab on the desired envelope, and drives the envelope into the capture region of the edge rollers. The edge rollers drive the envelope into the main rollers which drive the envelope and fiche into the projection gate. When the LED-photodiode edge sensor detects the first of several row fiducial marks on the film, selection is complete.

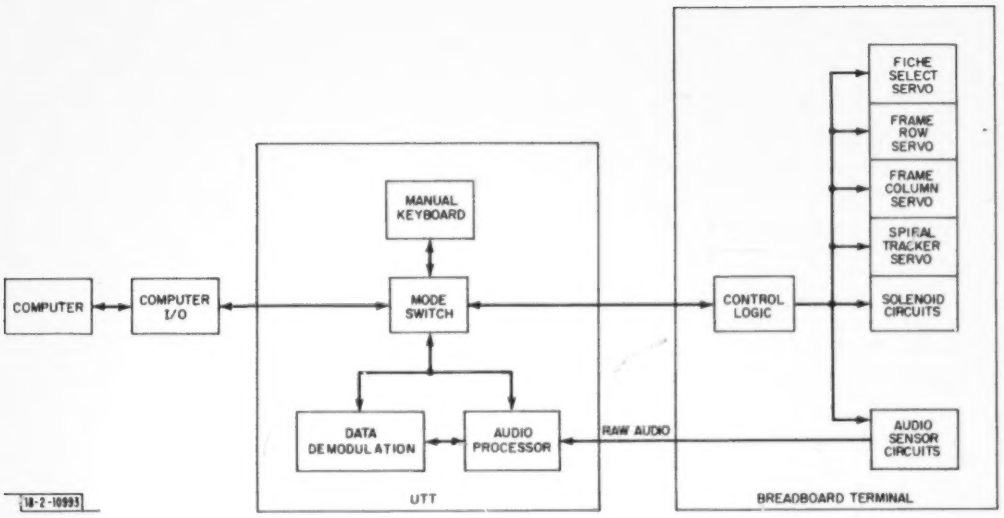

Fig. 3. Rotating microscope fiche selector/reader system.

Frame selection consists of separate, but parallel, activities. Row selection is achieved by open-loop slewing until the fiducial mark nearest the desired row is reached. The row servo loop is then closed, and the film is positioned by means of a null detector consisting of two LED-photodiode pairs and a fiducial mark.

Column selection is achieved by sensing and nulling to a code wheel attached to the column carriage cam, using pairs of LED-photodiodes.

When row and column selection has been completed, the registration pin is driven through the film, the projection gate is closed, and the spiral tracker is enabled.

The spiral tracker servo will resemble previous servos in most aspects, the key exception being the extra precision necessary when tracking at the film vs an enlarged image.

Five Light Emitting Diode Assemblies (LEDA) were received and acceptance tests conducted. Tests to determine peak radiance under proposed operating conditions will be made during the next quarter.

C. Self Processor Interface

The serial input (SERIN Branching Logic) interface to the SIM4-02 processor is complete and has been tested using data message lengths of 12 kilobits transmitted at rates up to 1800 bps.

Design of the remaining portions of the interface – fiche, frame and display control logic, interval timer logic, I/O flag control, keyboard strobe and display logic, and TTY I/O – was completed during this quarter, and construction of a complete system is under way.

The interface design is such that it will be compatible with existing LTS-3 student terminals as well as proposed new terminals including the LTS-3/S, the LTS-4, and the rotating microscope.

D. SIM4-02 I/O Software Development

A number of I/O software routines were developed and debugged during this quarter for use as system debugging aids, in the operating system, and as aids for system checkout.

1. SERIN Routine

The serial data input routine has been debugged, and operational tests with data message lengths of 12 kilobits at rates up to 1800 baud have been run satisfactorily.

2. TTY Communications Routines

Additions to SIM4-02 I/O software completed during the past quarter are as follows:

(a) TYIN Routine: Accepts inputs from the ASR33 TTY, converts input to 8 bit ASCII code, and loads into designated pair of processor index registers.

(b) TYOUT Routine: Outputs to ASR33 TTY (8-bit octal words held in a designated index register pair).

(c) STORE TTY: Stores 8-bit word data blocks from TTY keyboard or paper tape in designated area of RAM main memory. Block length and storage area initially set by operator via TTY.

(d) LIST TTY: Lists on TTY (8-bit words in octal) from designated area of RAM main memory. Memory area and list length preset by operator via TTY as with STORE routine.

(e) OCTBI Routine: Converts three octal characters, each held in separate 4-bit registers, to two 4-bit packed binary word pairs.

(f) BIOCT Routine: Converts 4-bit binary register pair to three separate octal characters. Note: OCTBI and BIOCT routines are used to pack TTY input for STORE and unpack TTY output for LIST.

III. LTS-3/S: STAND-ALONE MODEL OF LTS-3

During this quarter, we have started the conversion of an LTS-3 terminal to a stand-alone version (LTS-3/S) which will be used to support USAF lesson developments during FY 74-75 and for early evaluation of operational specifications for the LTS-4. Although it is likely that the microfiche format for the two systems will be different, we will make the individual frames compatible. Thus, the video and audio master frames can be used to compose either LTS-3/S clamped cards or LTS-4 cassette cards.

The modifications now under development to convert the existing LTS-3 terminals to stand-alone operation are listed below.

(a) Develop a SIM4-02 microprocessor to replace the PDP-8/I. This system has been under development for approximately one year, and the first version will be implemented during the Fall of 1973.

(b) Develop system software for the SIM4-02 to control the terminal. This effort is under way and is reported in Section I of this QTS.

(c) Develop a receive data modem for recovering the frame branching logic at the start of each frame. A modem has been developed and operated using an LTS-3 terminal and the recovered data processed by a SIM4-02. The long-term data error rate (Pe) has been less than 10^{-8}.

(d) Develop a hardware interface between the SIM4-02 and the terminal interface. A version of this interface has been constructed, and debugging is under way.

(e) Modify the audio modem to be compatible with LTS-4.

(f) Modify the coarse/vernier X-Y system to improve reliability and increase the acquisition range.

(g) Modify the radial tracker servo system to improve reliability and track acquisition range.

(h) Integrate the new subsystems into the LTS-3 cabinet.

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13. ABSTRACT

Work during this quarter has concentrated on further investigations of alternative designs for LTS-4 features and subsystems. A new film gate was designed and installed in the image rotator, and a new vernier positioning technique was implemented. Most of the parts for the rotating microscope selector/reader have been released for fabrication.

The self processor interface is nearing completion, and considerable progress has been made on system software utilizing the MCS-4 simulator. A new version of the author program language has been developed, and modifications of an LTS-3 to a stand-alone version for use in an author support facility are in progress.

14. KEY WORDS

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